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FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO. SP015.C17	APPLICATION NO. To Be Assigned
APPLICANT Nguyen et al.	
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			v.s.	PATENT DOCUMENTS					
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB - CLASS	FILING DATE		
i~	AA1	3,346,851	10/1967	Thornton et al.					
w	AB1	3,718,912	02/1973	Hasbrouck et al.					
N	AC1	3,771,138	11/1973	Celtruda et al.					
$a_{\underline{}}$	AD1	3,789,365	01/1974	Jen et al.					
~	AE1	4,034,349	07/1977	Monaco et al.					
n	AF1	4,200,927	04/1980	Hughes et al.					
	AG1	4,228,495	10/1980	Bernhard et al.					
n	AH1	4,296,470	10/1981	Fairchild et al.					
a	AI1	4,315,314	02/1982	Russo					
9	AJ1	4,410,939	10/1983	Kawakami					
	AK1	4,434,461	02/1984	Puhl					
			FOREIG	N PATENT DOCUMENTS			. •		
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION		
n	AL1	0 479 390 A2	08/1992	EP			Yes		
6	AM1	0 426 393	08/1991	EP			Yes		
6	AN1	0 419 105 A2	10/1990	EP			Yes No		
9	A01	0 402 856	12/1990	EP			Yes No		
0	AP1	0 377 991 A3	12/1989	EP			Yes		
		OTHER (Inc	luding Author,	Title, Date, Pertinent Pag	es, etc.)				
h	AR			er Handbook, Intel, 1989, p			-1 -3-37.		
5	Acosta, Raymond D. et al., "An Instruction Issuing Approach to Enhancing Performance in Multiple Functional Unit Processors," IEEE Transactions on Computers, Vol. C-35 No. 9, September 1986, pp. 815-828.								
4	AT	Agerwala Research	et al., "High Division, Marc	Performance Reduced Instructh 31, 1987, pp. 1-61.	tion Set	Processor	в," Івм		
EXAMINER	♣ ——,——— k		1		DATE CONS	idered	//		

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n	AA2	4,45	59,657	07/1984	м	urao					
n	AB2	4,47	76,525	10/1984	1	shii					
av.	AC2	4,62	26,989	12/1986	T	orii					
a	AD2	4,67	75,806	06/1987	υ	chida					
a	AE2	4,7	14,994	12/1987	0	klobdzija <i>et al</i> .					
a	AF2	T-	22,049	01/1988	L	ahti					
02	AG2	1	52,873	06/1988	s	honai et al.					
Cr	AH2	1	8,948	07/1988	т	ay et al.				<u> </u>	
6	AI2	1	56,566	08/1988		huang	 				
	AJ2	1	7,115	02/1989		orng	 		L		
~	AK2	1	8,105	08/1989	 	uriyama et al.	┢				
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2	AL2	0 37	72 751 A2	11/1989	Ε	P				Yes No	
1	AM2	0 36	58 332 A2	05/1990	E	P				Yes No	
~	AN2	0 35	54 585 A2	02/1990	Е	Р				Yes No	
2	AO2	0 17	71 595 A2	02/1986	E	p			·	Yes No	
	AP2	0 13	36 179 A2	09/1984	E	P				Yes No	
_		(OTHER (Incl	uding Author,	T	itle, Date, Pertinent Page	8,	etc.)			
. 4	AR	2		and Nicolau, i		, "Perfect Pipelining: A N	√ew	Loop P	aralleliz	ation	
	AS	<u>2</u>	Andrews, Distinctions Blur Between DSP Solutions, Computer Design, Vol. 28, No. 9, May 1, 1989, Littleton, Mass., pp. 86-99.								
4	AT	<u>2</u>	Charlesword Architecture 1981, pp.	ıral Design of	A t	pproach to Scientific Arra he AP-120B/FPS-164 Family,	ay P	rocess	ring: The	4, September	
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w	AA3	4,8	97,810	01/1990	Nix					
m	AB3	4,9	01,228	02/1990	Kodama					
90	AC3	4,9	01,233	02/1990	Liptay					
n	AD3	4,9	03,196	02/1990	Pomerene et al.					
4	AE3	4,9	24,376	05/1990	Ooi					
n	AF3	4,9	26,323	05/1990	Baror et al.					
h	AG3	4,9	42,525	07/1990	Shintani et al.					
m.	АН3	4,9	85,825	01/1991	Webb, Jr. et al.					
4	AI3	4,9	92,938	02/1991	Cocke et al.					
N	AJ3	5,0	03,462	03/1991	Blaner et al.					
N	AK3	5,1	01,341	03/1992	Circella et al.					
				FORBIG	N PATENT DOCUMENTS					
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a	AL3	2 5	75 564	12/1985	FR				Yes	
~	АМ З	2 0	11 682	11/1979	GB				Yes No	
n	AN3	61-	95447	06/1986	JР				Yes No	
Cr	A03	2-2	78337	11/1990	JP				Yes No	
1	AP3	3-1	37729	06/1991	JP				Yes No	
			OTHER (Inc.	uding Author,	Title, Date, Pertinent Pa	ges,	etc.)			
W	AR	<u>3</u>	Proceeding	as of the 2 nd]	Architecture for a Trace International Conference or Ind Operating Systems, Octo	n Arch	nitect	ural Suppo	rt for	
4	AS	3	Foster et Execution	al., "Percola ," IEEE Trans.	ation of Code to Enhance Pa On Computers, December 19	ralle	el Dis	patching a	nd	

Goodman, J.R. and Hsu, W., "Code Scheduling and Register Allocation in Large Basic Blocks," ACM, 1988, pp. 442-452. <u>3</u>

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ATTY. DOCKET NO. APPLICATION NO. SP015.C17 To Be Assigned FORM PTO-1449 APPLICANT Nguyen et al. INFORMATION DISCLOSURE STATEMENT FILING DATE GROUP Herewith To be assigned U.S. PATENT DOCUMENTS EXAMINER DOCUMENT INITIAL DATE NAME CLASS SUB-FILING DATE NUMBER CLASS N 5,127,091 02/1995 Horst AA4 2 AB4 5,129,067 07/1992 Johnson 7 AC4 5,134,561 07/1992 Liptay AD4 5,155,843 10/1992 Stamm et al. 9 AE4 5,187,796 02/1993 Wang et al. 07/1993 AP4 5,226,126 McFarland et al. 5,226,170 a AG4 07/1993 Rubinfeld 5,230,068 AH4 07/1993 Van Dyke et al. a AI4 5,355,460 10/1994 Eickenmeyer et al. Z McFarland et al. AJ4 5,442,757 08/1995 AK4 5,461,715 10/1995 Matsuo et al. FOREIGN PATENT DOCUMENTS EXAMINER INITIAL DOCUMENT DATE COUNTRY CLASS SUB-TRANSLATION NUMBER CLASS 3-147134 06/1991 JΡ Yes AL4 No 2-22736 01/1990 JΡ Yes AM4 No 2-87229 03/1990 JΡ Yes AN4 No 3-35322 02/1991 JР Yes A04 No 64-36366 02/1989 JP Yes AP4 No OTHER (Including Author, Title, Date, Pertinent Pages, etc.) Gross et al., "Optimizing Delayed Branches," Proceedings of the 5th Annual AR 4 Workshop on Microprogramming, October 5-7, 1982, pp. 114-120. Groves, R.D. and Oehler, R., "An IBM Second Generation RISC Processor AS 4 Architecture, " IEEE, 1989, pp. 134-137. Bakoglu et al., "IBM Second-Generation RISC Machine Organization," 1990, IERE, AT 4 pp. 173-178. EXAMINER DATE CONSIDERED EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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APPLICANT Nguyen et al.	
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W.	AA5	5,41	87,156	01/1996	Popescu et al.			
W	AB5	5,4	88,729	01/1996	Vesegna et al.			
~~·	AC5	5,5	39,911	07/1996	Nguyen et al.			
\sim	AD5	5,5	61,776	10/1996	Popescu et al.			
\sim	AE5	5,5	74,927	11/1996	Scantlin			
\mathcal{O}	AF5	5,5	92,636	01/1997	Popescu et al.			
	AG5	5,62	25,837_	04/1997	Popescu et al.			
9	AH5	5,6	27,983	05/1997	Popescu et al.			
Q)	AI5	5,6	51,125	07/1997	Witt et al.			
ω_{I}	AJ5	5,6	89,720	11/1997	Nguyen et al.			
	AK5	5,70	08,841	01/1998	Popescu et al.			
				FOREIG	N PATENT DOCUMENTS			
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\\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\	AL5	2-13	0634	05/1990	Japan			Yes No
	AM5							Yes No
	AN5						<u></u>	Yes No
	A05							Yes No
	AP5							Yes No
		(OTHER (Inc.	luding Author,	Title, Date, Pertiner	t Pages, etc.)		
() ()	AR	<u>21</u>	Hennessy	et al., Compu	O Mflops 64-bit Microps -15.2.4. ter Architecture: A Qua (in its entirety).			7
0	AT	<u>5</u>	Horst, R.V	W. et al., "M ," IEEE, 1990	ultiple Instruction Is: , pp. 216-226.		/	ne
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CN _	AA6	5,70	68,575	06/1998	М	cFarland et al.				
Top .	AB6	5,7	78,210	07/1998	н	enstrom et al.				
Ev.	AC6	5,79	97,025	08/1998	P	opescu et al.				
a	AD6	5,8	32,205	11/1998	ĸ	elly et al.				
	AE6	5,8	32,293	11/1998	P	opescu et al.				
4	AF6	5,9	61,629	10/1999	N	guyen et al.				
1	AG6	6,0	38,654	03/2000	N	guyen et al.				
9	AH6	6,0	92,181	07/2000	1	guyen et al.				
w	AI6		01,594	08/2000	1	guyen et al.				
9/	AJ6		28,723	10/2000	1	guyen et al.	<u> </u>			
7	AK6	T	33,694	08/1993	Т	otta et al.			 	
	AKO	3,2	33,054	<u> </u>			<u> </u>		I	<u> </u>
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, ,	AL6	<u> </u>								Yes No
	AM6									Yes No
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	AP6				Ī					Yes No
		•	OTHER (Incl	uding Author	'-	itle, Date, Pertinent Page		eta)		
W	AR	<u>6</u>	Hwu et al	., "HPSm, a Hi Inctionality,"	igh	Performance Restricted Daroceedings from ISCA-13,	ata	Flow A	Architectu Dan, June	re Having 2-5, 1986,
\mathcal{N}	Hwu et al., "Checkpoint Repair for High-Performance Out-of-Order Execution Machines," IEEE Trans. On Computers, Vol. C-36, NO. 12, December 1987, pp. 1496-1514.									
4	AT	<u>6</u>	Compiler (., "Exploiting Code Generator are, June 1988	: , "	arallel Microprocessor Mic Proceedings of the 15 th A pp. 45-53.	croa	rchite	ectures wi	th a Computer
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	AL7								Yes No	
	AM7				·				Yes No	
	AN7								Yes No	
	A07	ļ							Yes No	
	AP7								Yes No	
			OTHER (Incl	uding Author,	Title, Date, Pertinent	Pages,	atc.)			
W	AR	7	IBM Journa	al of Research	and Development, Vol. 3	4, No.	l, Jan	uary 1990	, pp. 1-70.	
\mathcal{N}	AS	7	Succeeding	M Technical Disclosure Bulletin, Overlap of Store Multiple Operation With cceeding Operations through Second Set of General Purpose Registers, Voll 28, 6, November 1989, New York, NY, pp. 2727-2728.						
	ĀŦ	7	Jelemensky Applicatio CA, pp. 51	ons, Electro C	mputer Features Advanced onference Record, Vol. 1	Hardwa	re For l 11,	Real-Tim 1989, Los	e Control Angeles,	
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	AM8								Yes
	AN8								Yes
	АОВ								Yes
	AP8								Yer No
	<u> </u>		OTHER (Incl	uding Author,	Title, Date, Pertinent I	Pages,	etc.)		
W	AR	8		Villiam M., St	uper-Scalar Processor Des			tation),	copyright
0	AS	8	Johnson, N	William M., Su ety).	uper-Scalar Processor Des	ign, Pr	rentic	е-Hall, I	nc., 1991 (in
	AT	<u>8</u>	Jouppi, N	H., "Integrated, pp. 229-232	tion and Packaging Plateat	us of I	Proces	sor Perfe	rmance,"
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	AN9								Yes No	
	A09								Yes No	
	AP9								Yes No	
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W	AR	9	Parallelis	em and Its Eff	uniform Distribution of In Fect on Performance," IEEE 989, pp. 1645-1658.	struct Trans	tion-Le saction	evel and M ns on Comp	achine uters, Vol.	
1	AS	<u>9</u>	Superpipel Architectu	ouppi et al., "Available Instruction-Level Parallelism for Superscalar and uperpipelined Machines," Proceedings of the 3 rd International Conference on rchitectural Support for Programming Languages and Operating Systems, April 989, pp. 272-282.						
1	AT	<u>9</u>	Keller, R. 1975, pp.	.M., "Look-Ahe	ead Processors," Computing	Surve	eys, Vo	ol, 7, No	4, December	
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	AN10						 		No Yes
	A010								Yes
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	· ·		OTHER (Incl	uding Author,	Title, Date, Pertin	ent Pages,	etc.)		
	AR	10	Lam, M.S., Comput. So	"Instruction ci., Vol. 4, 1	Scheduling For Supe	erscalar Ar	chitect	cures," Ar	nnu. Rev.
\mathcal{A}	AS	<u>10</u>	Lee, Ruby	B., "Precisio	n Architecture," CON	1PUTER, Ja n	uary 19	989, pp. 7	78-91.
1	AT	10	Melear, C. 9, No. 2,	, Motorola, I April 1989, L	nc., The Design of toos Alamitos, CA, pp.	the 88000 R	ISC Fam	nily, IEEE	MICRO, Vol.
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	AM11							Yes				
	AN11							Ye:				
	A011							Yes				
	AP11							Yes				
			OTHER (Incl	uding Author,	Title, Date, Pertinent	Pages, etc.)						
h)	AR	11	Murakami, Pipelining 78-85.	K. et al., "S)): A Novel Hi	IMP (Single Instruction gh-Speed Single-Process	n Stream/Multi sor Architectu	ple Instr re," ACM,	uction 1989, pp.				
A)	AS	11	Workstatio	dnert, D. et al., "Architecture and Compiler Enhancements for PA-RISC orkstations," Proceedings from IEEE Compcon, February 25-March 1, 1991, San rancisco, CA, pp. 214-218.								
W	AT	11	Patent Abs	atent Abstracts of Japan, Vol. 010, No. 089, April 1986, & JP, A, 60 225 943 Hitachi Seisakusho K K) November 11, 1985.								
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AR	12	Microarch:	itecture," Pro	ceedings of the 18 th A	A High Perform	ance on Microp	rogramming,			
AS	<u>12</u>	Patt et a. Proceeding 103-108.	Patt et al., "HPS, A New Microarchitecture: Rationale and Introduction," Proceedings of the 18 th Annual Workshop on Microprogramming, December 1985, pp. 03-108.							
AT	12	Processor	s," Proceeding	Performance Potential of the 15 th Annual S	of Multiple Fund	ctional Un	nit hitecture,			
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	AR	<u>13</u>	Pleszkun e the 14 th Ir	et al., "WISQ: nternational S	A Restartable Architectur ymposium on Computer Arch	re Usi itectu	ng Que ire, Ju	ues," Pro ine 1987,	oceedings of pp. 290-299.		
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	,AT	<u>13</u>	S. McGeady	S. McGeady, "The i960A Superscalar Implementation of the 80960 Architecture," IEEE, 1990, pp. 232-240.							
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U	AT	14	Smith et al., "Limits on Multiple Instruction Issue," Proceedings of the 3rd International Conference on Architectural Support for Programming Languages and Operating Systems, April 1989, pp. 290-302									
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9	AS	<u>15</u>	Sohi, Gurindar S. and Sriram Vajapeyam, "Instruction Issue Logic for High-Performance, Interruptable Pipelined Processors," Conference Proceedings of the 14 th Annual International Symposium on Computer Architecture, June 2-5, 1987, pp. 27-34.								
)	AT	<u>15</u>	Thornton, J.E., Design of a Computer: The Control Data 6600, Control Data Corporation, 1970, pp. 58-140.								
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U	AT	<u>20</u>	Kuga Morihiro et al., "Low-Level Parallel Processing Algorithm for the SIMP Processor Prototype," Department of Information Systems, Interdisciplinary Graduate School of Engineering Sciences, Kyushu University, Vol. 30, No. 12, Dec. 1987, pp. 1603-1611.						
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INFORMATION DISCLOSURE STATEMENT

Page 2 of 2 ATTY. DOCKET NO. SP015.C17 (1397.028000H) 10/7
FIRST NAMED INVENTOR: NGUYEN et al. APPLICATION NO. 10/700,485

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Page 1 of 1 APPLICATION NO. ATTY, DOCKET NO. 10/700,485 SP015.C17 (1397.028000H) **FORM PTO-1449** FIRST NAMED INVENTOR: NGUYEN et al. INFORMATION DISCLOSURE STATEMENT FILING DATE **ART UNIT** November 5, 2003 2183 **U.S. PATENT DOCUMENTS** DOCUMENT **EXAMINER** CLASS SUB-CLASS INITIA NUMBER DATE NAME FILING DATE AA8 4,901,233 02/13/1990 Liptay 07/28/1992 5,134,561 AB8 Liptay 12/05/1995 AC8 5,473,764 Chi AD8 DADEMARK AE8 AF8 AG8 AH8 NE AI8 AJ8 AK8 **FOREIGN PATENT DOCUMENTS EXAMINER** INITIAL **DOCUMENT** DATE COUNTRY CLASS SUB-CLASS **TRANSLATION** NUMBER 64 36336 02/07/1989 Japan Yes AL7 No Yes AM7 No Yes AN7 No Yes **AO7** No Yes AP7 No OTHER (Including Author, Title, Date, Pertinent Pages, etc.) <u>31</u> AS <u>31</u> Final Rejection, mailed January 30, 2004, for Japanese Appl. No. 2000-146443, and English language translation of same, 3 pages... AT <u>31</u> **EXAMINER** DATE CONSIDERED **EXAMINER:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant. 244562_1.DOC SKGF Rev. 12/03/03

Page 1 of 1 APPLICATION NO. ATTY. DOCKET NO. 10/700,485 SP015.C17 (1397.028000H) **FORM PTO-1449** FIRST NAMED INVENTOR: NGUYEN et al. Fifth Supplemental

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ATTY. DOCKET NO.
SP015.C17 (1397.028000H)
FIRST NAMED INVENTOR: NGUYEN et al.

APPLICATION NO. 10/700,485

Page 2 of 2

Sixth Supplemental
INFORMATION DISCLOSURE STATEMENT

FILING DATE November 5, 2003

ART UNIT 2183

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0/	AE9	6,647,485	11/2003	Nguyen et al.			
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Page 1 of 2 ATTY. DOCKET NO. APPLICATION NO. 10/700,485 SP015.C17 (1397.028000H) FORM PTO-1449 FIRST NAMED INVENTOR: NGUYEN et al. venth Supplemental ON DISCLOSURE STATEMENT FILING DATE ART UNIT November 5, 2003 2183 **U.S. PATENT DOCUMENTS** DOCUMENT **EXAMINER** INITIAL NUMBER DATE NAME CLASS SUB-CLASS **FILING DATE** AA9 AB9 AC9 AD9 AE9 5,167,035 AF9 11/1992 Mann et al. AG9 2003-0056086-3/20/2003 Nguyen et al. AH9 2003-0079113-4/24/2003 Nguyen et al. Α1 2003-0070060-Al9 4/10/2003 Nguyen et al. A1 2003-0056087-3/20/2003 AJ9 Nguyen et al. AK9 2004-0054872-3/18/2004 Nguyen et al. A1 FOREIGN PATENT DOCUMENTS **EXAMINER** INITIAL **DOCUMENT** DATE COUNTRY **CLASS** SUB-CLASS **TRANSLATION** NUMBER Yes AL8 No Yes 8MA No Yes **8NA** No Yes 80A No Yes AP No OTHER (Including Author, Title, Date, Pertinent Pages, etc.) AR <u>33</u> AS <u>33</u> AT <u>33</u> **EXAMINER** DATE CONSIDERED **EXAMINER**: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line/through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant. 363983_1.DOC SKGF Rev. 12/03/03

FORM PTO-1449
Seventh Supplemental
INFORMATION DISCLOSURE STATEMENT

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